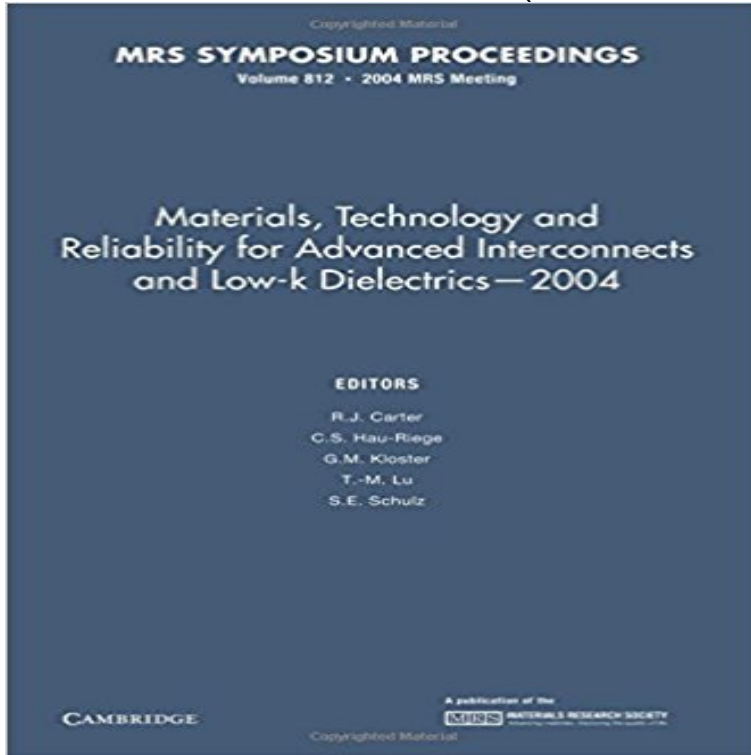


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The scaling of device dimensions with a simultaneous increase in functional density has imposed tremendous challenges for materials, technology, integration and reliability of interconnects. To meet requirements of the ITRS roadmap, new materials are being introduced at a faster pace in all functions of multilevel interconnects. The issues addressed in this book cannot be dispelled as simply selecting a low-k material and integrating it into a copper damascene process. The intricacies of the back end for sub-100nm technology include novel processing of low-k materials, employing pore-sealing techniques and capping layers, introducing advanced dielectric and diffusion barriers, and developing novel integration schemes. This is in addition to concerns of performance, yield, and reliability appropriate to nanoscaled interconnects. Although many challenges continue to impede progress along the ITRS roadmap, the contributions in this book confront them head-on. It provides a scientific understanding of the issues and stimulate new approaches to advanced multilevel interconnects.

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